

IN THE CLAIMS:

Claims 1-10, 12-14, and 17-31 have been amended herein. All of the pending claims 1 through 31 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Original) A method for polishing or planarizing a surface of a semiconductor device structure, comprising:
selectively applying a plurality of different amounts of pressure to different, selected locations of
a backside of the semiconductor device structure; and
polishing or planarizing at least one layer on the surface of the semiconductor device structure.
2. (Currently Amended) The method of claim 1, wherein ~~the~~ selectively applying the plurality of different amounts of pressure comprises biasing independently movable pressurization structures against the backside of the semiconductor device structure.
3. (Currently Amended) The method of claim 2, wherein ~~the~~ biasing comprises magnetically biasing the independently movable pressurization structures against the backside.
4. (Currently Amended) The method of claim 3, wherein ~~the~~ magnetically biasing comprises magnetically repelling the independently movable pressurization structures toward the backside.
5. (Currently Amended) The method of claim 3, wherein ~~the~~ magnetically biasing comprises magnetically attracting the independently movable pressurization structures toward the backside.
6. (Currently Amended) The method of claim 2, wherein ~~the~~ biasing comprises resiliently biasing the independently movable pressurization structures against the backside.

7. (Currently Amended) The method of claim 6, wherein ~~the~~ selectively applying comprises selectively applying a negative pressure to at least one of the independently movable pressurization structures.

8. (Currently Amended) The method of claim 2, wherein ~~the~~ biasing comprises applying a positive pressure to at least one of the independently movable pressurization structures.

9. (Currently Amended) The method of claim 1, wherein ~~the~~ polishing or planarizing comprises chemical-mechanical polishing.

10. (Currently Amended) The method of claim 1, wherein ~~the~~ selectively applying a plurality of different amounts of pressure and the polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure.

11. (Original) The method of claim 1, further comprising locating at least one raised area on an active surface of the semiconductor device structure.

12. (Currently Amended) The method of claim 11, wherein ~~the~~ selectively applying a plurality of different amounts of pressure comprises applying an appropriate amount of pressure to the backside of the semiconductor device structure, opposite the at least one raised area ~~thereof~~ so as to planarize the active surface during the polishing or planarizing.

13. (Currently Amended) The method of claim 11, wherein ~~the~~ selectively applying a plurality of different amounts of pressure comprises selectively applying pressure to a backside of another semiconductor device structure of the same type as the semiconductor device structure, opposite a location of the at least one raised area of the semiconductor device structure.

14. (Currently Amended) The method of claim 13, wherein ~~the~~ polishing or planarizing comprises forming a substantially planar surface on the semiconductor device structure.

15. (Original) The method of claim 1, comprising substantially simultaneously applying the plurality of different amounts of pressure to the backside of the semiconductor device structure.

16. (Original) A method for polishing at least one layer on a semiconductor device structure, comprising:
polishing at least one layer of a first semiconductor device structure;
locating any raised areas on the first semiconductor device structure following the polishing;
selectively applying pressure to a backside of at least one second semiconductor device structure of a same type as the first semiconductor device structure, the selectively applying being effected at locations beneath areas of the at least one second semiconductor device structure that correspond to the raised areas of the first semiconductor device structure;
and
at least mechanically polishing at least one layer of the at least one second semiconductor device structure.

17. (Currently Amended) The method of claim 16, wherein ~~the~~ locating comprises employing metrology techniques.

18. (Currently Amended) The method of claim 16, wherein ~~the~~ selectively applying comprises applying a sufficient amount of pressure at each of the locations to form a substantially planar surface on the at least one second semiconductor device structure.

19. (Currently Amended) The method of claim 16, wherein ~~the~~ selectively applying comprises selectively applying different amounts of pressure at different ones of the locations.

20. (Currently Amended) The method of claim 16, wherein ~~the~~ selectively applying comprises determining an appropriate amount of pressure to apply to each of the locations based on a height of each corresponding raised area.

21. (Currently Amended) The method of claim 16, wherein ~~the~~ selectively applying comprises selectively applying pressure to the backside of the at least one second semiconductor device structure ~~at~~ to at least one annular location.

22. (Currently Amended) The method of claim 16, wherein ~~the~~ polishing comprises mechanically polishing the at least one layer of the first semiconductor device structure.

23. (Currently Amended) The method of claim 16, wherein ~~the~~ polishing comprises chemical-mechanical polishing the at least one layer of the first semiconductor device structure.

24. (Currently Amended) The method of claim 16, wherein ~~the~~ at least mechanically polishing comprises chemical-mechanical polishing the at least one layer of the at least one second semiconductor device structure.

25. (Currently Amended) The method of claim 16, wherein ~~the~~ selectively applying comprises biasing at least one pressurization structure against the backside of the at least one second semiconductor device structure.

26. (Currently Amended) The method of claim 25, wherein ~~the~~ biasing comprises employing a magnet to bias the at least one pressurization structure against the backside.

27. (Currently Amended) The method of claim 26, wherein ~~the~~ employing the magnet comprises repelling the at least one pressurization structure toward the backside to effect ~~the~~ biasing.

28. (Currently Amended) The method of claim 26, wherein ~~the~~ employing the magnet comprises attracting the at least one pressurization structure toward the backside to effect ~~the~~ biasing.

29. (Currently Amended) The method of claim 25, wherein ~~the~~ biasing comprises resiliently biasing ~~at the~~ at least one pressurization structure against the backside.

30. (Currently Amended) The method of claim 29, wherein ~~the~~ selectively applying further comprises applying a negative pressure to the at least one pressurization structure.

31. (Currently Amended) The method of claim 25, wherein ~~the~~ biasing comprises applying a selected amount of positive pressure to the at least one pressurization structure.